## CLAIMS

1. An emitter, comprising:

an electron supply;

a cathode layer; and

a tunneling layer disposed between the electron supply and the cathode layer wherein the electron supply, cathode layer, and tunneling layer have been subjected to an annealing process..

2. The emitter of claim 1 wherein the tunneling layer is a metal cluster dielectric.

3. The emitter of claim 1 wherein the tunneling layer is a metal cluster dielectric selected from the group consisting of $TiO_x$, $TaO_x$, WSiN, $TaAlO_xN_y$, $TaAlO_x$ and $AlO_xN_y$.

4. The emitter of claim 1 wherein the cathode layer is selected from the group consisting of platinum, gold, molybdenum, tantalum, iridium, ruthenium, chromium, and alloys thereof.

5. The emitter of claim 1 operable to provide an emission current of greater than $1 \times 10^{-2}$ Amps per square centimeter.

6. The emitter of claim 1 operable to provide an emission current of greater than $1 \times 10^{-1}$ Amps per square centimeter.

7. The emitter of claim 1 operable to provide an emission current of greater than 1 x 10 Amps per square centimeter.

8. The emitter of claim 1wherein the tunneling layer has a thickness less than about 500 Angstroms.

9. The emitter of claim 1 wherein the tunneling layer has a thickness less than about 250 Angstroms.

10. The emitter of claim 1 wherein the tunneling layer has a thickness less than about 100 Angstroms.

11. The emitter of claim 1 wherein the tunneling layer has a thickness of about 50 Angstroms.

12. The emitter of claim 1 wherein the tunneling layer has a thickness within the range of about 50 to about 250 Angstroms.

13. An integrated circuit, comprising:

a substrate;

the emitter of claim 1 disposed on the substrate; and

circuitry for operating the emitter formed on the substrate with the emitter.

14. An electronic device, comprising:

the emitter of claim 1 capable of emitting energy; and

an anode structure capable of receiving the emitted energy and generating at least a first effect in response to receiving the emitted energy and a second effect in response to not receiving the emitted energy.

15. The electronic device of claim 14 wherein the electronic device is a mass storage device and the anode structure is a storage medium, the electronic device further comprising a reading circuit for detecting the effect generated on the anode structure.

16. The electronic device of claim 14 wherein the electronic device is a display device and the anode structure is a display screen that creates a visible effect in response to receiving the emitted energy.

17. The electronic device of claim 16 wherein the display screen includes one or more phosphors operable for emitting photons in response to receiving the emitted energy.

18. A storage device, comprising:

at least one emitter to generate an electron beam current, wherein the at least one emitter has been subjected to an annealing process;

a lens for focusing the electron beam current to create a focused beam; and

a storage medium in close proximity to the at least one emitter, the storage medium having a storage area being in one of a plurality of states to represent the information stored in that storage area;

such that:

an effect is generated when the focused beam bombards the storage area;

the magnitude of the effect depends on the state of the storage area; and

the information stored in the storage area is read by measuring the magnitude of the effect.

19. The storage device of claim 18 wherein the effect is a signal current.

20. The storage device of claim 18 wherein the emitter has a tunneling layer less than 500 Angstroms.

21. An emitter, comprising:

an electron supply layer;

an insulator layer formed on the electron supply layer and having an opening defined within;

a tunneling layer formed on the electron supply layer in the opening; and

a cathode layer formed on the tunneling layer;

wherein the emitter has been subjected to an annealing process to increase the supply of electrons tunneled from the electron supply layer to the cathode layer for energy emission.

22. The emitter of claim 21 capable of emitting photons in addition to the electron emission.

23. The emitter of claim 21 wherein the tunneling layer is a metal cluster dielectric.

24. The emitter of claim 21 wherein the cathode layer has an emission rate greater than about 0.01 Amps per square centimeter.

25. The emitter of claim 21 wherein the tunneling layer is a metal cluster dielectric selected from the group consisting of $TiO_x$, $TaO_x$, WSiN, $TaAlO_xN_y$, $TaAlO_x$ and $AlO_xN_y$.

26. The emitter of claim 21 wherein the tunneling layer has a thickness less than 500 Angstroms.

27. The emitter of claim 21 wherein the tunneling layer has a thickness between about 50 Angstroms and about 250 Angstroms.

28. A display device, comprising:

an integrated circuit including the emitter of claim 21, wherein the emitter emits a visible light source; and

a lens for focusing the visible light source, wherein the lens is coated with a transparent conducting surface to capture electrons emitted from the emitter.

29. A storage device, comprising:

an integrated circuit including the emitter of claim 21 wherein the emitter creates an electron beam current; and

a storage medium in close proximity to the emitter, the storage medium having a storage area being in one of a plurality of states to represent the information stored in that storage area;

such that:

an effect is generated when the electron beam current bombards the storage area;

the magnitude of the effect depends on the state of the storage area; and

the information stored in the storage area is read by measuring the magnitude of the effect.

30. An electronic device, comprising:

an integrated circuit including the emitter of claim 21; and

a focusing device for converging the emissions from the emitter.

31. A computer system, comprising:

a microprocessor;

the electronic device of claim 30 coupled to the microprocessor; and

memory coupled to the microprocessor, the microprocessor operable of executing instructions from the memory to transfer data between the memory and the electronic device.

32. The computer system of claim 31 wherein the electronic device is a storage device.

33. The computer system of claim 31 wherein the electronic device is a display device.

34. An emitter, comprising:

an electron supply surface;

an insulator layer formed on the electron supply surface and having a first opening defined within;

an adhesion layer disposed on the insulator layer, the adhesion layer defining a second opening aligned with the first opening;

a conductive layer disposed on adhesion layer and defining a third opening aligned with the first and second openings;

a tunneling layer formed on the electron supply layer within the first, second, and third openings; and

a cathode layer disposed on the tunneling layer and portions of the conductive layer, wherein the portion of the cathode layer on the tunneling layer is an electron-emitting surface.

35. The emitter of claim 34 wherein the electron emitting surface has an emission rate of about 0.1 to about 1.0 Amps per square centimeter.

36. The emitter of claim 34, wherein the tunneling layer is a metal cluster dielectric film from the group consisting of $TaO_x$, WSiN, $TiO_x$, $TaAlO_xN_y$, $TaAlO_x$, and $AlO_xN_y$.

37. The emitter of claim 34, wherein the tunneling layer has a thickness between about 50 Angstroms to about 250 Angstroms.

38. The emitter of claim 34, wherein the tunneling layer has a thickness of about 100 Angstroms.

39. The emitter of claim 34, wherein the tunneling layer has a thickness less than about 500 Angstroms.

40. The emitter of claim 34 wherein the electron-emitting surface also emits photon energy.

41. An emitter, comprising:

an emitting surface having a first area;

a first chamber having substantially parallel sidewalls interfacing to the emitting surface; and

a second chamber interfacing to the first chamber and having sidewalls diverging to an opening having a second area larger than the first area.

42. The emitter of claim 41, further comprising a cathode layer disposed on the emitting surface, and sidewalls of the first and second chambers and wherein the emitter has been subjected to an annealing process thereby increasing the emission capability of the emitter.

43. The emitter of claim 41 wherein the first chamber is formed within an adhesion layer.

44. The emitter of claim 41 wherein the second chamber is formed within a conductive layer.

45. An integrated circuit comprising at least one emitter of claim 41.

46. A display device comprising at least one emitter of claim 41.

47. A storage device comprising at least one emitter of claim 41.

48. An integrated circuit, comprising:

a conductive surface to provide an electron supply;

at least one emitter formed on the electron supply including,

an insulator layer having at least one opening to define the location and shape of the at least one flat emitter device,

a conductive layer disposed over the insulator layer, the conductive layer having at least one opening in alignment with the at least one opening;

a tunneling layer disposed within the at least one opening of the insulator layer; and

a cathode layer disposed over the tunneling layer and partially over the conductive layer.

49. The integrated circuit of claim 48 wherein the tunneling layer is a metal cluster dielectric.

50. The integrated circuit of claim 48 wherein the tunneling layer has a thickness less than about 500 Angstroms.

51. The integrated circuit of claim 48 wherein the tunneling layer has a thickness between about 50 Angstroms and about 250 Angstroms.

52. The integrated circuit of claim 48 wherein the tunneling layer is $TiO_x$.

53. The integrated circuit of claim 48 wherein the tunneling layer is a metal cluster dielectric selected from the group consisting of $TaO_x$, WSiN, $TaO_xN_y$, $TaAlO_xN_y$, $TaAlO_x$, and $AlO_xN_y$.

54. The integrated circuit of claim 48 wherein the integrated circuit has been subjected to an annealing process.

55. A method for creating an emitter on an electron supply, comprising the steps of:

forming a tunneling emitter using semiconductor thin-film layers on the electron supply, at least one of the thin-film layers being a film characterized as a tunneling layer with a thickness of less than 500 Angstroms.

56. An emitter created by the process of claim 55.

57. The method of claim 55 further comprising the step of annealing the processed emitter to increase the tunneling current of the tunneling emitter.

58. The method of claim 55 wherein the step of applying the tunneling layer further comprises the step of applying a metal cluster dielectric.

59. The method of claim 55 wherein the step of forming the tunneling layer further comprises the step of applying a metal cluster dielectric for the tunneling dielectric from the group consisting of $TiO_x$, $TaO_x$, WSiN, $TaAlO_xN_y$, $TaAlO_x$, and $AlO_xN_y$.

60. The method of claim 55 wherein the applied tunneling layer has a thickness between about 50 Angstroms and about 250 Angstroms.

61. The method of claim 55 further comprising the step of applying a cathode layer on the tunneling layer.

62. A method for creating an emitter on an electron supply, comprising the steps of:

applying a conductive layer to adhere to an insulator layer disposed on the electron supply, the insulator layer defining an opening to the electron supply;

applying a patterning layer on the conductive layer;

creating an opening in the patterning and conductive layer to the electron supply;

applying a tunneling layer over the patterning layer and the opening; and

etching the patterning layer to remove it from under the tunneling layer thereby removing the tunneling layer not disposed in the opening by lift-off from the conductive layer.

63. An emitter created by the process of claim 62.

64. The method of claim 62 further comprising the step of annealing the processed emitter to increase the tunneling current.

65. The method of claim 62 wherein the applied tunneling layer has a thickness less than about 500 Angstroms.

66. The method of claim 62 further comprising the step of applying a cathode layer on the tunneling layer.

67. A method for creating an emitter on an electron supply surface, the method comprising the steps of:

creating an insulator layer on the electron supply surface;

defining an emission area within the insulator layer;

applying an adhesion layer on the insulator layer;

applying a conduction layer on the adhesion layer;

applying a patterning layer on the conduction layer;

creating an opening to the conduction layer in the patterning layer;

etching the conduction layer in the opening to the adhesion layer;

etching the adhesion layer to the electron supply;

applying a tunneling layer over the patterning layer and the opening;

etching the patterning layer beneath the tunneling layer and thereby lifting off the tunneling layer except a portion adhered to the electron supply surface in the opening;

applying a cathode layer over the portion of the tunneling layer and a portion of the conduction layer; and

etching the cathode layer.

68. An emitter created by the process of claim 67

69. The method of claim 67 further comprising the step of annealing the processed emitter.

70. The method of claim 67 wherein the applied tunneling layer has a thickness less than 500 Angstroms.

71. The method of claim 67 wherein the applied tunneling layer has a thickness within the range of about 50 to about 250 Angstroms.